Remarks

With regard to paragraphs 1 and 2 of the Office action, claims 1 and 3-10 are under consideration. Claims 11-30 are withdrawn without traverse.

With regard to paragraph 3 of the Office action the drawings were objected to for not showing every feature of the invention specified in the claims. The last sentence of the Background Art section of the application reads as follows: "An object of the invention is to provide a semiconductor memory array having mostly non-volatile memory cells but with permanently written data in portions of the memory array." Memory arrays are well understood in chip technology. For example, in the book "Semiconductor Memories" by A. Sharma, IEEE Press (1997) on pages 47 and 207, copy attached as Exhibit A, memory arrays are represented by empty boxes. The same is true in hundreds, perhaps thousands, of U.S. patents. In other words, memory arrays are so well understood by persons skilled in the art that there is no point in illustrating details of a memory array. Nevertheless, to achieve compliance with the rule cited by the Examiner, Applicant has added Fig. 7 to show a memory array, i.e., rows and columns of memory cells that have been mentioned in the specification. The array of Fig. 7 is now further described by this amendment in the Brief Description of the Drawings and in the specification at the beginning of the Description and at the end of the Description. No new matter has been added because the array itself and groups of rows within the array were previously described in the specification.

With regard to paragraphs 4 and 5 of the Office action, claim 1 was rejected under 35 U.S.C. § 112 for failing to show how different types of memory are integrated or configured. The Examiner suggests that sub-arrays are a part of Applicant's invention. With all due respect, Applicant

does not contemplate sub-arrays or any particular type of configuration. Memory cells of the same type exist in rows, as disclosed in the specification on page 6, beginning at line 27. The reason for grouping in rows is explained. Apart from grouping similar types of transistors in rows, no separate treatment within a memory array is required. The same addressing circuitry, power supply and so on is used. Since each memory device has an associated sense device, each transistor may be addressed separately and read separately. The configuration issues suggested by the Examiner simply do not exist and so there is no need for discussion.

With regard to paragraphs 6 and 7 of the Office action, claim 3 was rejected for use of the term "common electrode" in each memory cell. The term "common electrode" should be "shared electrode" and so the term has been amended. The shared electrode is, for example, shared drain 55 described in the specification on page 6, line 12 and with reference to Fig. 2, shared drain 23 described on page 4, lines 27 and 28. The shared drain is the only shared electrode and is shown in Figs. 2, 4, and 6. Claim has been corrected to change the word "common" to -- shared --.

It is noted that no prior art has been cited against the application, pursuant to the Examiner's discussion in paragraphs 8-11 of the Office action.

Conclusion

Applicant has addressed the issues raised by the Examiner under 35 U.S.C. 112. No new matter has been added. All amendments have clear support in the specification. From the title of the invention, it is seen that Applicant is showing and describing use of a single mask set to produce read-only elements in a non-volatile transistor memory array. The last phrase of claim 1 states: "the non-volatile memory cells and the read-only memory cell having the same footprint within a single memory array." This limitation highlights a novel and non-obvious invention which merits a patent.

Reconsideration of the claims is requested in view of this amendment and remarks herein. A Notice of Allowance is earnestly solicited.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) on the date shown below.

Signed: /Sally Azevedo/
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Date: February 1, 2008

Respectfully submitted,

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